KAWASAKI
LSI

KCUSB3

USB Controller – Quick Interface

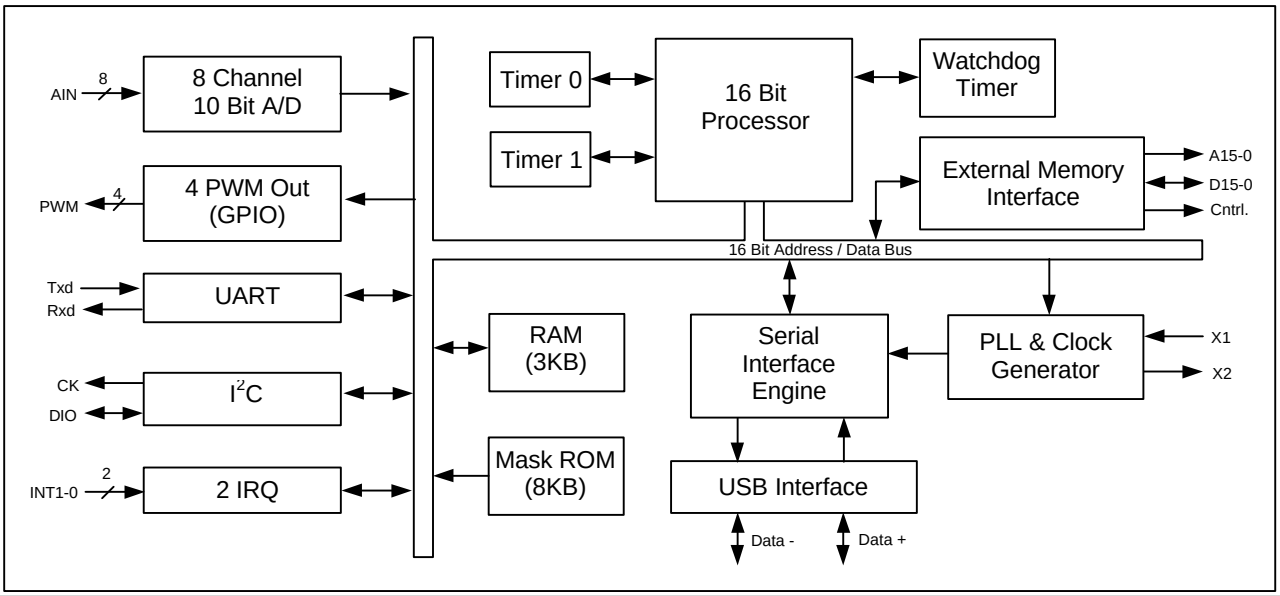
General Description

The Kawasaki KCUSB3 Controller is a quick single chip solution to interface peripheral devices to the Universal Serial Bus (USB). The KCUSB3 has been specifically designed to provide a simple and fast method of designing interfaces for peripheral devices to the USB port. This has been accomplished by its highly integrated functionality and flexible General Purpose I/O (GPIO) that can be configured to your system requirements. This device has been configured with a wide range of capabilities for your immediate use or evaluation. The device can then be reconfigured for your specific application. You can directly access the embedded processor's address and data lines to use external programmable logic for evaluation before configuring the GPIO for your final device. The SIE (Serial Interface Engine) is fully compatible with the USB specification.

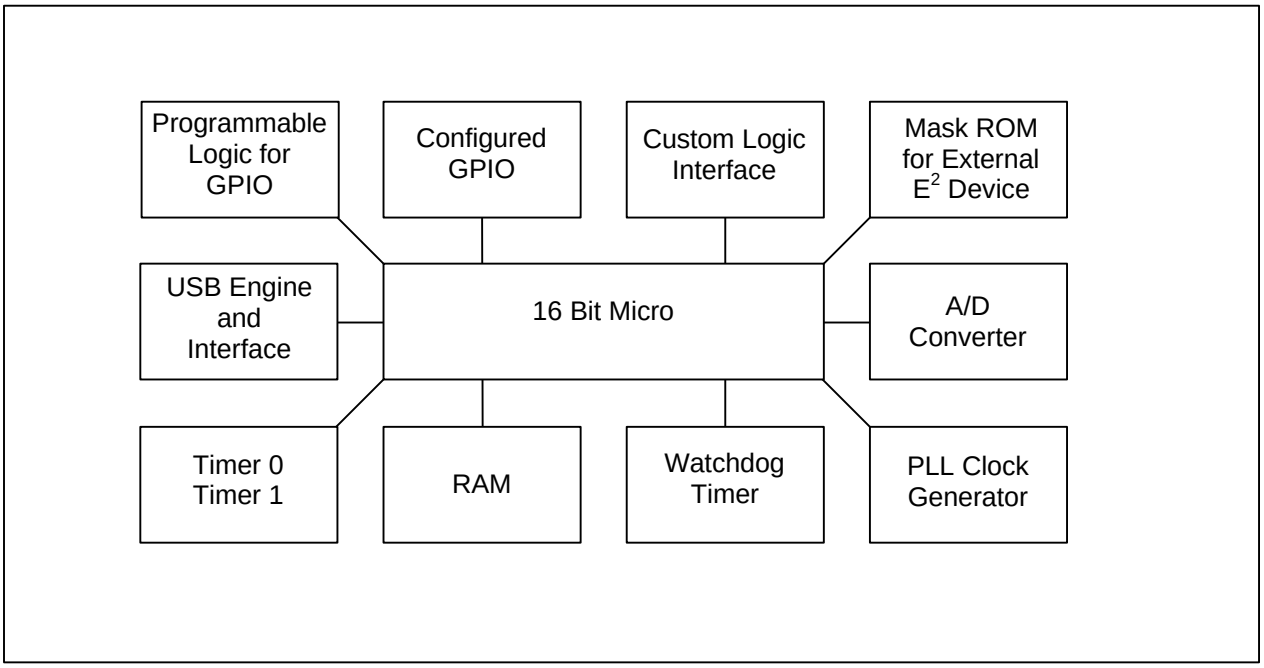
Features

- Advanced 16 Bit processor for USB transaction processing and control data processing
- USB interface ver 1.0/1.1 compliant
- Transceivers and SIE (Serial Interface Engine)
- Internal Clock Generation
- Utilizes low cost external crystal circuitry
- 1.5K x 16 Internal RAM buffer
- 2 IRQ
- 8 Channel, 10 Bit A/D
- External Memory Interface for direct access to the 16-bit processor for using external logic or memory.
- General purpose I/O
- Watchdog timer
- PWM Output Support
- 8K user programmable gates
- 8K bytes ROM
- I^2C Interface
- 100 pin QFP package

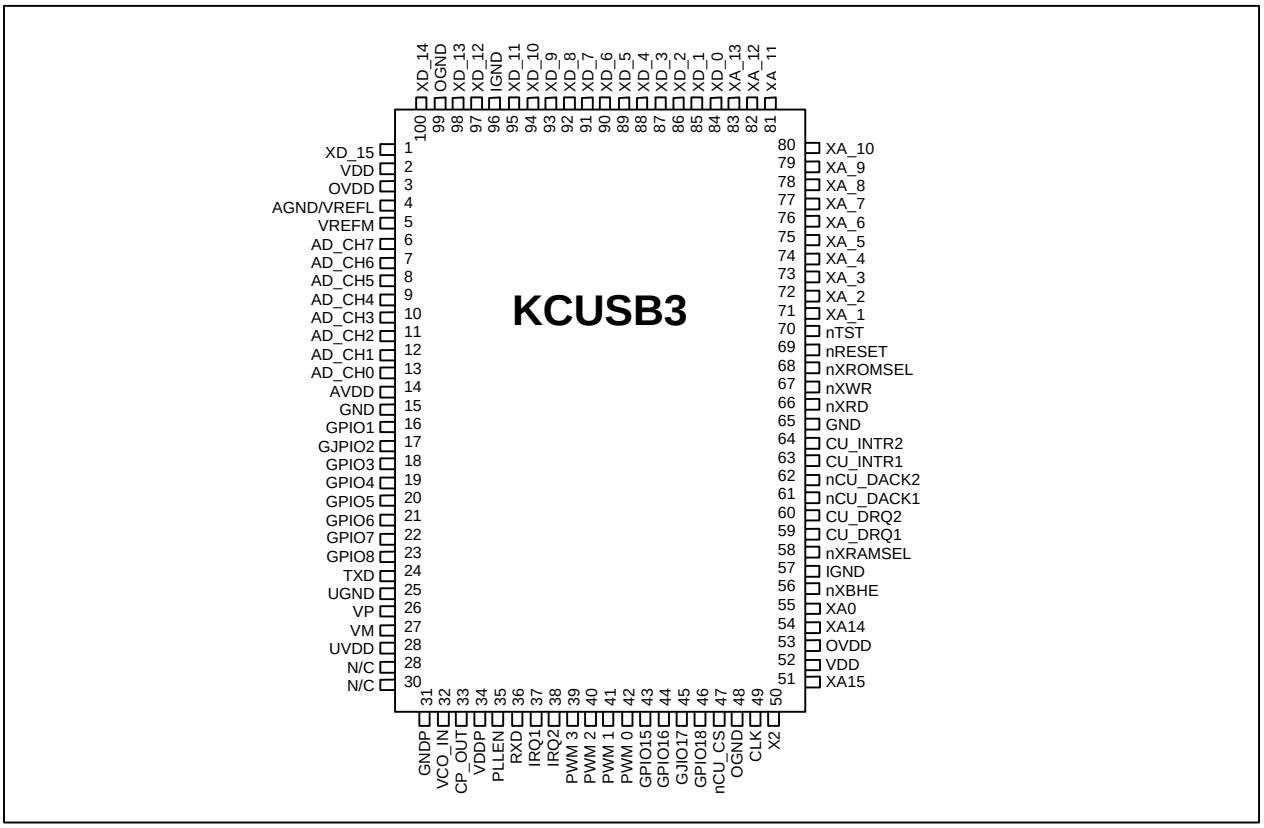
Block Diagram (Application Example)



KCUSB3 Basic Blocks



Pin Diagram



Pin Description

Pin Number	I/O	Pin Name	Description	Programmable I/O Mode *
1	IN/OUT	XD_15	External Data Pins	
2	IN	VDD	VDD	
3	IN	OVDD	VDD	
4	IN	AGND/VREFL	Analog GND	
5	OUT	VREFM	AD converter reference	
6	IN	AD_CH7	A/D Converter Input	
7	IN	AD_CH6	A/D Converter Input	
8	IN	AD_CH5	A/D Converter Input	
9	IN	AD_CH4	A/D Converter Input	
10	IN	AD_CH3	A/D Converter Input	
11	IN	AD_CH2	A/D Converter Input	
12	IN	AD_CH1	A/D Converter Input	
13	IN	AD_CH0	A/D Converter Input	
14	IN	AVDD	Analog VDD	
15	IN	GND	GND	
16	IN/OUT	GPIO1	General GPIO	GPIO1
17	IN/OUT	GPIO2	General GPIO	GPIO2
18	IN/OUT	GPIO3	General GPIO	GPIO3
19	IN/OUT	GPIO4	General GPIO	GPIO4
20	IN/OUT	GPIO5	General GPIO	GPIO5
21	IN/OUT	GPIO6	General GPIO	GPIO6
22	IN/OUT	GPIO7	General GPIO	GPIO7
23	IN/OUT	GPIO8	General GPIO	GPIO8
24	OUT	TXD	UART TXD	
25	IN	UGND	USB GND	
26	IN/OUT	VP	USB + Pin	
27	IN/OUT	VM	USB – Pin	
28	IN	UVDD	USB VDD	
29	NC	NC	NC	
30	NC	NC	NC	
31	IN	GNDP	GND	
32	IN	VCO_IN	PLL VCO_IN	
33	OUT	CP_OUT	PLL VCO Out	
34	IN	VDDP	VDD	
35	IN	PLLEN	PLL Enable	
36	IN	RXD	UART RXD	
37	IN	IRQ1	Edge sens. Interrupt	GPIO9
38	IN	IRQ2	Edge sens. Interrupt	GPIO10
39	OUT	PWM3	Pulse Width Modulator 3	GPIO11
40	OUT	PWM2	Pulse Width Modulator 2	GPIO12
41	OUT	PWM1	Pulse Width Modulator 1	GPIO13
42	OUT	PWM0	Pulse Width Modulator 0	GPIO14
43	IN/OUT	GPIO15		GPIO15
44	IN/OUT	GPIO16		GPIO16
45	IN/OUT	GPIO17		GPIO17

Pin Number	I/O	Pin Name	Description	Programmable I/O Mode *
46	IN/OUT	GPIO18		GPIO18
47	IN/OUT	nCU_cs	Custom Logic Chip_Select	GPIO19
48	IN	OGND	GND	
49	IN	CLK	12MHz Clock/Crystal Input	
50	OUT	X2	12MHz Crystal Output	
51	OUT	XA_15	External Address Pins	
52	IN	VDD	VDD	
53	IN	OVDD	VDD	
54	OUT	XA_14	External Address Pins	
55	OUT	XA0	External Address Pin	
56	OUT	nXBHE	External byte High Enable (Active low)	
57	IN	IGND	GND	
58	OUT	nXRAMSEL	External RAM CS (Active low)	
59	IN/OUT	CU_DRQ1	Custom Logic DMA Rq#1	GPIO20
60	IN/OUT	CU_DRQ2	Custom Logic DMA Rq#2	GPIO21
61	IN/OUT	nCU_DACK1	Custom Logic DMA Ack#1	GPIO22
62	IN/OUT	nCU_DACK2	Custom Logic DMA Ack#2	GPIO23
63	IN/OUT	CU_INTR1	Custom Logic Intreq #1	GPIO24
64	IN/OUT	CU_INTR2	Custom Logic Intreq #2	GPIO25
65	IN	GND	GND	
66	OUT	nXRD	External Memory Read (Active low)	
67	OUT	nXWR	External Memory Write (Active low)	
68	OUT	nXROMSEL	External ROM CS (Active low)	
69	IN	nRESET	Reset Pin	
70	IN	nTST	Test Pin, *Disconnect for Normal Operation*	
71	OUT	XA_1	External Address Pin	
72	OUT	XA_2	External Address Pin	
73	OUT	XA_3	External Address Pin	
74	OUT	XA_4	External Address Pin	
75	OUT	XA_5	External Address Pin	
76	OUT	XA_6	External Address Pin	
77	OUT	XA_7	External Address Pin	
78	OUT	XA_8	External Address Pin	
79	OUT	XA_9	External Address Pin	
80	OUT	XA_10	External Address Pin	
81	OUT	XA_11	External Address Pin	
82	OUT	XA_12	External Address Pin	
83	OUT	XA_13	External Address Pin	
84	IN/OUT	XD_0	External Data Pins	
85	IN/OUT	XD_1	External Data Pins	
86	IN/OUT	XD_2	External Data Pins	
87	IN/OUT	XD_3	External Data Pins	
88	IN/OUT	XD_4	External Data Pins	
89	IN/OUT	XD_5	External Data Pins	
90	IN/OUT	XD_6	External Data Pins	
91	IN/OUT	XD_7	External Data Pins	
92	IN/OUT	XD_8	External Data Pins	
93	IN/OUT	XD_9	External Data Pins	

Pin Number	I/O	Pin Name	Description	Programmable I/O Mode *
94	IN/OUT	XD_10	External Data Pins	
95	IN/OUT	XD_11	External Data Pins	
96	IN	IGND	GND	
97	IN/OUT	XD_12	External Data Pins	
98	IN/OUT	XD_13	External Data Pins	
99	IN	OGND	GND	
100	IN/OUT	XD_14	External Data Pins	

* Dedicated GPIO's are not selected.

Function Description

16 Bit Processor

The integrated 16 bit processor serves as a micro controller for USB peripherals. The processor can execute approximately five million instructions per second. With this processing power it allows the design of intelligent peripherals that can process data prior to passing it on to the host PC, thus improving overall performance of the system. The masked ROM (4K X 16) in the KCUSB3 or external memory contains a specialized instruction set that has been designed for highly efficient coding of processing algorithms and USB transaction processing.

The 16-bit processor is designed for efficient data execution by having direct access to the RAM Buffer, external memory, I/O interfaces, and all the control and status registers. The divide/multiply feature expands the capability of USB peripherals.

The processor contains sixteen general-purpose registers along with several special purpose registers including a flag register and an interrupt enable register. Eight of these registers can be used for indirect Addressing, with optional indexed and auto increment modes available. One of these general-purpose registers is additionally used as a stack pointer. The register set is mapped into RAM, and can be easily relocated for fast context switching.

The processor supports prioritized vectored hardware interrupts. In addition, as many as 240 software interrupt vectors are available.

The processor provides six addressing modes, supporting memory-to-memory, memory-to-register, register-to-register, immediate-to-register or immediate-to-memory operations. Register, direct, immediate, indirect, and indirect indexed addressing modes are supported. In addition, there is an auto-increment mode in which a register, used as an address pointer is automatically incremented after each use, making repetitive operations more efficient both from a programming and a performance standpoint.

The processor features a full set of program control, logical, and integer arithmetic instructions. All instructions are sixteen bits wide, although some instructions require operands, which may occupy another one or two words. Several special " short immediate" instructions are available, so that certain frequently used operations with small constant operand will fit into a 16-bit instruction.

The Processor – Divide/Multiply function

The processor's divide/multiply function contains all the instructions of the base processor that additionally includes integer divide and multiply instructions. A signed multiply instructions takes two 16-bit operands and returns a 32-bit result. A signed divide instruction divides a 32-bit operand by a 16-bit operand.

RAM Buffer

The USB controller contains a 3K byte (1.5K X 16) internal buffer memory. The memory is used to buffer data and USB packets and accessed by the 16 Bit processor and the SIE. USB transactions are automatically routed to the memory buffer. The 16-bit processor has the ability to set up pointers and block sizes in buffer memory for USB transactions. Data is read from the interface and is processed and packetized by the 16-bit I/O processor.

PLL Clock Generator

The PLL circuitry is provided to generate the internal 48MHz clock requirements. This circuitry is designed to allow use of a low cost 12 MHz external crystal which is connected to the KCUSB3 pins X1 and X2. If an external 12 MHz clock is available in the application, it may be used in lieu of the crystal circuit and connected directly to the X1 input pin.

USB Interface

The USB controller meets the Universal Serial Bus (USB) specification ver 1.0. The transceiver is capable of transmitting and receiving serial data at the USB's full speed, 12 Mbits/sec data rate. The driver portion of the transceiver is differential, while the receive section is comprised of a differential receiver and two single ended receivers. Internally, the transceiver interfaces to the SIE logic. Externally, the transceiver connects to the physical layer of the USB.

A/D interface

The integrated A/D interface is a ten bit A/D interface with eight Analog Inputs and converts data at 100K samples per second.

PWM Interface

Four PWM output channels are available with each channel capable of converting 10 bits at a rate up to 48 KHz.

UART Interface

Supports a transfer rate of 900 to 115.2K baud.

General Purpose I/O

Up to 25 general purpose I/O signals are available. Most of the GPIOs can be configured for special purpose functions such as PWM, Serial EEPROM interface, Digital Input, etc.

Serial EEPROM Support

The USB Controller serial interface is used to provide access to external EEPROM's. The interface is implemented using General Purpose I/O signals and can support a variety of serial EEPROM formats.

Custom Logic Interface

The internal 16 bit data and address bus is connected to the Custom Logic block allowing custom logic to interface to the processor and to access a selection of GPIO pins.

Development Tools

To assist in the development of USB products, an evaluation board is available as well as a set of software tools and debuggers. Compilers and debuggers are available through third party suppliers.

Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD5}	-0.6 to 6.0	V
	V_{DD}	-0.3 to 4.0	V
Input Voltage	V_{IN} (Normal)	-0.6 to V_{DD5}+0.6	V
		-0.3 to V_{DD}+0.3	V
	V_{IN} (5V Tolerant)	-0.3 to 7.3	V
DC Output Current	I_{OUT}	±30 *	mA
Storage Temperature	TSTG	-55 to 125 **	°C

*24mA buffers
**Plastic Package

DC Characteristics and conditions (V_{DD5} @ 3V±.3V)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
V_{DD5}	Supply Voltage	-	3.0	3.3	3.6	V
V_{IH}	Input high voltage	CMOS	2.15	-	-	V
V_{IL}	Input low voltage	CMOS	-	-	0.95	V
V+	Input high voltage	TTL Schmitt		1.32	1.75	V
		CMOS Schmitt		2.17	2.65	V
V-	Input low voltage	TTL Schmitt	0.45	0.86	-	V
		CMOS Schmitt	0.50	1.03	-	V
V_H	Hysteresis voltage	TTL Schmitt	0.25	-	-	V
		CMOS Schmitt	0.56	-	-	V
I_{IH}	Input high current	$V_{IN} = V_{DD5}$	-10	-	10	µA
I_{IL}	Input low current	$V_{IN} = V_{ss}$	-10	-	10	µA
V_{OH}	Output high voltage	I_{OH} = -4mA	2.4	-	-	V
V_{OL}	Output low voltage	I_{OL} = 4mA	-	-	0.4	V
I_{OZ}	3-state leakage current	$V_{OL}=V_{DD5}$	-10	-	10	µA
		$V_{IN}=V_{SS}$	-12	-34	-100	µA

*IDDS is design dependent